IN THE SPECIFICATION

On page 5 of Amendment A, please delete the first paragraph.

On page v of the marked-up version of Amendment A, please delete the second full paragraph.

Please amend the paragraph beginning at line 8 of page 47 as follows:

In servicing the interrupt a physical page (or pages if the interrupt is used to allocate a whole texture rather than just a page) must be allocated by software. If these physical pages are already assigned then the corresponding logical pages must be marked as nonresident [[non resident]] in the Logical Texture Page Table. If these newly nonresident [[non resident]] logical pages are subsequently accessed (maybe by a queued texture operation) they themselves will cause a page fault and be reassigned. [[re assigned.]] Hence no knowledge of what textures are waiting in the DMA buffer to be used is necessary. The physical pages are allocated from the host working set whose base page is given by BaseOfWorkingSetHost register.

Please amend the paragraph beginning at line 29 of page 50 as follows:

Figure 4B shows actions in the Primary Cache Manager. If a cache miss occurs (test 421), the details of the missing texel are obtained (step 423), and the next free cache line is looked up (step 425). A read command is then issued to the address generator (step 429), [[427),]] specifying the free cache line as the return address. The address generator updates the T

FIFO after the read request has occurred. A message is then written into the M FIFO with details of the cache lines used, fragment details, and the number (if any) of additional cache loads which have now occurred.

B2 Cont

Please amend the paragraph beginning at line 15 of page 75:

According to certain disclosed embodiments there is provided: A graphics processing method, comprising the steps of: (a.) caching texture memory fetches, using a cache tag assignment which is essentially unique mapped, while (b.) generating condensed cache tags, by removing two bits from the tag length by means of a remapping which exploits the different address resolutions implied by level of detail settings in the different mip mapping processes to re-encode the mip mapping addresses ~~corresponding to said cache tag assignment, by combining a mip mapping level of detail parameter which can have at least $2^{J+1}+1$ different values together with coordinate bits which can have as many as 2^{K} different values into fewer than J + K bits without loss of information~~ (c.) and using said condensed tags for said caching step (a.).

B3